PATENT
Attorney Docket No: MAGMA-00702

Amendments to the Specification:

Please replace the paragraph at Page 7, Lines 3-19 with the following rewritten paragraph:

An apparatus for reducing a throughput time of a processing path of basic logic elements within an integrated circuit, the apparatus comprising a programming module for programming a first substitute circuit into the processing path of the integrated circuit, wherein the substitute circuit is not defined by a sequence of basic Boolean circuits and, ~~and~~ wherein the substitute circuit is defined by a truth table identical to a truth table defining a processing path comprised of basic Boolean circuits. The apparatus further comprising a circuit generation module configured to analyze a sequence of basic Boolean elements and generate a complimentary substitute circuit. According to an embodiment, the processing path comprises an input flip flop. According to an embodiment, the integrated circuit is an NMOS circuit. In an embodiment of the present invention, the apparatus further comprises a sequence generator for generating a plurality of sequences of Boolean elements, wherein the circuit generation module is configured to generate a complimentary substitute circuit for each sequence of Boolean elements generated, a library for storing the plurality of sequences of Boolean elements such that each Boolean element is stored in a correlation to its complimentary substitute circuit, a search module for searching the library for a first sequence of Boolean elements, and a retrieval module for retrieving a substitute circuit from the library. In an embodiment, the library comprises a digital medium.